REMARKS

By this amendment, claim 30 have been amended. Accordingly, claims 18, 30, 31 and 33-35 are currently pending in the application, of which claims 18 and 30 are independent claims.

In view of the above amendments and the following Remarks, Applicants respectfully request reconsideration and timely withdrawal of the pending rejections for the reasons discussed below.

Examiner Interview

Applicants appreciate that the Examiner granted the interview on January 30, 2004. This response is prepared based on the discussion during the interview.

Rejections Under 35 U.S.C. §103

In the Office Action, claims 18, 30, 31, 34 and 35 have been rejected under 35 U.S.C. §103(a) for being unpatentable over U. S. Patent No. 5,259,881 issued to Edwards, *et al.* ("Edwards") in view of U. S. Patent No. 5,198,694 issued to Kwasnick, *et al.* ("Kwasnick") and further in view of U. S. Patent No. 5,578,520 issued to Zhang, et al. ("Zhang"). This rejection is respectfully traversed.

It is submitted that the claims of the present application have been amended several times and are now very specifically reciting claimed features. Particularly, independent claims 18 and 30 specifically recite each chamber's target object and process to be performed.

For example, claim 18 recites:

> "18. An apparatus for depositing a layer on a substrate for a liquid crystal device, comprising:
> a load lock chamber receiving *a substrate having a gate wire pattern* formed thereon;
> a preheat chamber receiving the substrate from said load lock chamber and heating the substrate before deposition;
> a deposition chamber depositing *a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon layer by chemical vapor deposition*; and
> a sputter chamber depositing a metal layer on the doped amorphous silicon layer by sputtering,
> wherein the substrate is transferred from said deposition chamber to said sputter chamber in a vacuum, and
> wherein said load lock chamber, said preheat chamber, said deposition chamber and said sputter chamber are arranged in series."

As such, independent claim 18 specifically recites "a load lock chamber receiving *a substrate having a gate wire pattern formed thereon*". Thus, it is prerequisite to form a gate wire pattern on the substrate before the substrate is processed by the claimed apparatus.

In this regard, the Examiner admitted "The difference between Edwards et al. and the present claims is that utilizing the chambers for forming layers of a thin film transistor is not discussed". Regarding this missing claimed features, the Examiner asserted Kwasnick discloses, in Figs. 1-6, "a layer of gate metallization 18 is disposed across the entire upper surface of the illustrated portion of the substrate 12" and "a gate dielectric layer 28 ... a layer 30 of intrinsic amorphous silicon ... a layer 32 of n+ amorphous silicon ... deposited ... without breaking the vacuum in the deposition chamber" (Office Action, pages 5-6).

However, Kwasnick is directed to a method of fabricating an LCD device, not an apparatus that is used for LCD fabrication. There is no teaching or suggestion as to an apparatus used for the processing steps described therein and elements (e.g., chambers) constituting the apparatus. Thus, it would not have been possible for one skilled in the art to conceive from

Kwasnick that a gate wire pattern in formed on a substrate before the substrate is received to an apparatus.

Similarly, claim 18 specifically recites "a deposition chamber depositing a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon layer by chemical vapor deposition". This means "a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon layer" are deposited *in a single deposition chamber specifically by chemical vapor deposition.*

In this regard, Kwasnick merely describes "a gate dielectric layer 28 ... a layer 30 of intrinsic amorphous silicon ... a layer 32 of n+ amorphous silicon ... deposited ... without breaking the vacuum in the deposition chamber", but one skilled in the art would not have been conceived that these layers are formed in a single chamber. Rather, he would have concluded that these layers have been formed in different chambers since Edwards discloses a substrate is transformed among different chambers without breaking a vacuum.

As explained so far, the combination of Edwards and Kwasnick does not disclose the very specific functions that are performed by each chambers described in claim 18. Also, as explained above, it would not have been obvious for a person with ordinary skilled in the art to come up with the claimed apparatus which receives a substrate having a gate wire pattern already formed thereon and has a single deposition chamber depositing a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon layer by chemical vapor deposition.

Similarly, independent claim 30 recites "a load lock chamber for receiving a substrate having a gate wire pattern formed thereon". As previously mentioned, Edwards and Kwasnick do not disclose or suggest this specific limitation.

Independent claim 30 also recites "a first deposition chamber for depositing a gate insulating layer and an amorphous silicon layer on the gate wire pattern; a second deposition chamber for depositing a doped amorphous silicon layer on the substrate". As previously mentioned, Edwards does not disclose the details of the jobs performed by the chambers, and Kwasnick is not directed to an apparatus used for the process steps described therein.

For these reasons, it is respectfully submitted that claims 18 and 30 are patentable over Edwards, Kwasnick and Zhang. Claims 31, 34 and 35 that are dependent from claim 30 would be also patentable at least for the same reasons. Accordingly, Applicants respectfully request that the rejection over claims 18, 30, 31, 31, 34 and 35 be withdrawn.

Claims 18, 30, 31 and 33-35 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U. S. Patent No. 5,512,320 issued to Turner, et al. ("Turner") in view of Kwasnick. This rejection is respectfully disagreed with.

Turner is directed to a method of depositing sequential thin film on glass substrates by a single vacuum deposition chamber processing. The vacuum system of Turner comprises a plurality of process chambers and heating/cooling chambers.

However, Turner does not disclose the specific detailed performed by each chambers recited in claims 18 and 30. For example, independent claim 18 "a load lock chamber receiving *a substrate having a gate wire pattern formed thereon*". This means a gate wire pattern is formed on the substrate before the substrate is received by the apparatus. Turner does not disclose or suggest that the apparatus shown in Fig. 1 satisfies this claimed feature.

Also, Turner describes "The processing chamber 40, 42, 44 and 46 are adopted to deposit one or more thin layers onto the glass substrate" but does not meet the specific details described

in claim 18, For example, claim 18 recites "a deposition chamber depositing a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon layer by chemical vapor deposition". Turner does not point out a specific chamber designated for "depositing a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon layer by chemical vapor deposition", as claimed.

As previously mentioned, the secondary reference to Kwasnick is directed to the process steps for fabricating an LCD device but does not capable of disclosing or even implying these missing claimed features from Turner because there is no description as to an apparatus used for the process steps and its structure.

Thus, the combination of Turner and Kwasnick does not disclose the very specific functions that are performed by each chambers described in claim 18. Also, as explained above, it would not have been obvious for a person with ordinary skilled in the art to come up with the claimed apparatus which receives a substrate having a gate wire pattern already formed thereon and has a single deposition chamber depositing a gate insulating layer, an amorphous silicon layer and a doped amorphous silicon layer by chemical vapor deposition.

Similarly, independent claim 30 recites "a load lock chamber for receiving a substrate having a gate wire pattern formed thereon". As previously mentioned, Turner and Kwasnick do not disclose or suggest this specific limitation.

Independent claim 30 also recites "a first deposition chamber for depositing a gate insulating layer and an amorphous silicon layer on the gate wire pattern; a second deposition chamber for depositing a doped amorphous silicon layer on the substrate". As previously mentioned, Turner does not disclose the details of the jobs performed by the chambers, and Kwasnick is not directed to an apparatus used for the process steps described therein.

For these reasons, it is respectfully submitted that claims 18 and 30 are patentable over Turner and Kwasnick. Claims 31 and 33-35 that are dependent from claim 30 would be also patentable at least for the same reasons. Accordingly, Applicants respectfully request that the rejection over claims 18, 30, 31 and 33-35 be withdrawn.

Other Matters

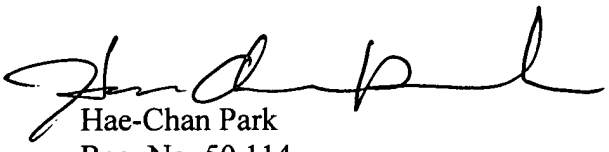
In this response, claim 30 has been amended to correct an antecedent basis error. Claim 30 recites "a first deposition chamber for depositing a gate insulating layer and an amorphous silicon layer on *the gate wire pattern*" but there was no "a gate wire pattern" in claim 30. To correct this error, claim 30 has been amended to recite "a load lock chamber for receiving a substrate having *a gate wire pattern formed thereon*".

CONCLUSION

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, claims 18, 30, 31 and 33-35 are in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,



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